It is claimed:

1. A method comprising:

providing a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions;

executing a first instruction of said plurality of instructions which generates a first register value for a first real register, said first register value being stored in a first alias register identified in a first entry of said reorder buffer associated with said first instruction; and

determining whether said first register value should be copied from said first alias register to said first real register approximately at a time when said first entry of said reorder buffer is needed for a second instruction that is younger in order than said first instruction.

2. The method of claim 1, asserting a first valid data field of said first entry of said reorder buffer after said execution of said first instruction but before said determining whether said first register value should be copied from said first alias register to said first real register, said asserted first valid data field indicates that said first register value is valid for copying from said first alias register to said first real register.

3. The method of claim 2, further comprising reading said first valid data field in determining whether said first register value should be copied from said first alias register to said first real register.

4. The method of claim 3, further comprising copying said first register value from said first alias register to said first real register if said first valid data field indicates that said first register value is valid for copying into said first real register.

5. The method of claim 2, further comprising deasserting a second valid data field of a second entry of said reorder buffer, said second entry including a second alias register previously associated with said first real register, said deasserted second valid data field indicates that said second register value is not valid for copying from said second alias register to said first real register.

6. The method of claim 1, further comprising:

providing a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry of said data commitment table comprising a committed data location field to indicate if a second register value generated by a third instruction is stored in a second alias register or in said first real register, and a reorder buffer index field to identify a second entry of said reorder buffer containing said second alias register if said second register value is stored in said second alias register;

determining whether said second register value is in said second alias register or in said first real register by reading said committed data location field of said data commitment table;

deasserting a second valid data field of said second entry of said reorder buffer if it is determined that said second register value is in said second alias register, said deasserted indicates that said second register value is not valid for copying from said second alias register to said first real register; and

writing an identifier for said first entry of said reorder buffer in said reorder buffer index field of said first entry of said data commitment table.

7. A processor system comprising:

a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions;

an execution unit to execute a first instruction of said plurality of instructions which generates a first register value for a first real register, said execution causing said first register value to be stored in a first alias register identified in a first entry of said reorder buffer associated with said first instruction; and

an allocator to add new instructions into said reorder buffer, said allocator determining whether said first register value should be copied from said first alias register to said first real register approximately at a time when said allocator determines that said first entry of said reorder buffer is needed for a second instruction that is younger in order than said first instruction.

8. The processor system of claim 7, further comprising a retirement unit to assert a first valid data field of said first entry of said reorder buffer after said execution unit has executed said first instruction but before said allocator determines whether said first register value should

be copied from said first alias register to said first real register, said asserted first valid data field indicates that said first register value is valid for copying from said first alias register to said first real register.

9. The processor system of claim 8, wherein said allocator reads said first valid data field in determining whether said first register value should be copied from said first alias register to said first real register.

10. The processor system of claim 9, wherein said allocator causes a copying of said first register value from said first alias register to said first real register if said first valid data field indicates that said first register value is valid for copying into said first real register.

11. The processor system of claim 8, wherein said retirement unit causes a deasserting of a second valid data field of a second entry of said reorder buffer, said second entry identifying a second alias register previously associated with said first real register, said deasserted second valid data field indicates that said second register value is not valid for copying from said second alias register to said first real register.

12. The processor system of claim 7, further comprising:

a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry of said data commitment table comprising a first committed data location field to indicate if a second register value generated by a third instruction is stored in a second alias register associated with said first real register or in said first real register, and a reorder buffer index field to identify a second entry of said reorder buffer identifying said second alias register if said second register value is stored in said second alias register;

wherein said retirement unit determines whether said second register value is in said second alias register or in said first real register by reading said first committed data field of said data commitment table;

wherein said retirement unit causes a deasserting of a second valid data field of said second entry of said reorder buffer if said retirement unit determines that said second register value is in said second alias register, said deasserted indicates that said second register value is not valid for copying from said second alias register to said first real register; and

and wherein said retirement unit causes a writing of an identifier for said first entry of said reorder buffer in said buffer index field of said first entry of said data commitment table.

13. A computer readable medium comprising one or more software modules to:

generate a reorder buffer containing a plurality of entries associated respectively with a plurality of instructions;

execute a first instruction of said plurality of instructions which generates a first register value for a first real register, said first register value being stored in a first alias register identified in a first entry of said reorder buffer associated with said first instruction; and

determine whether said first register value should be copied from said first alias register to said first real register approximately at a time when said first entry of said reorder buffer is needed for a second instruction that is younger in order than said first instruction.

14. The computer readable medium of claim 13, wherein said one or more software modules to further assert a first valid data field of said first entry of said reorder buffer after said execution of said first instruction but before said determining whether said first register value should be copied from said first alias register to said first real register, said asserted first valid data field indicates that said first register value is valid for copying from said first alias register to said first real register.

15. The computer readable medium of claim 14, wherein said one or more software modules to further cause a reading of said first valid data field in determining whether said first register value should be copied from said first alias register to said first real register.

16. The computer readable medium of claim 15, wherein said one or more software modules to further cause a copying of said first register value from said first alias register to said first real register if said first valid data field indicates that said first register value is valid for copying into said first real register.

17. The computer readable medium of claim 14, wherein said one or more software modules to further cause a deasserting of a second valid data field of a second entry of said reorder buffer, said second entry including a second alias register previously associated with said

first real register, said deasserted second valid data field indicates that said second register value is not valid for copying from said second alias register to said first real register.

18. The computer readable medium of claim 13, wherein said one or more software modules to further:

provide a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry of said data commitment table comprising a committed data location field to indicate if a second register value generated by a third instruction is stored in a second alias register or in said real register, and a reorder buffer index field to identify a second entry of said reorder buffer containing said second alias register if said second register value is stored in said second alias register;

determine whether said second register value is in said second alias register or in said first real register by reading said committed data location field of said data commitment table;

deassert a second valid data field of said second entry of said reorder buffer if it is determined that said second register value is in said second alias register, said deasserted indicates that said second register value is not valid for copying from said second alias register to said first real register; and

write an identifier for said first entry of said reorder buffer in said reorder buffer index field of said first entry of said data commitment table.

19. A method, comprising:

providing a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions including a first entry associated with a first instruction, said first entry identifying a first alias register containing a first register value for a first real register;

identifying said first entry of said reorder buffer to be associated with a second instruction that is younger in order than said first instruction;

determining whether said first register value is valid for copying from said first alias register to said first real register;

copying said first register value from said first alias register to said first real register if it is determined that said first register value is valid; and

associating said first entry of said reorder buffer with said second instruction.

20. The method of claim 19, wherein said first entry of said first instruction includes a first valid data field to indicate whether said first register value is valid for copying from said first alias register to said first real register, and wherein determining whether said first register value is valid comprises reading said first valid data field.

21. The method of claim 20, further comprising deasserting said first valid data field after determining that said first register value is valid for copying from said first alias register to said first real register.

22. The method of claim 19, further comprising:

providing a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry including a committed data location field to indicate whether a committed register value is in said first real register; and

asserting said data location field after it is determined that said first register value is valid for copying from said first alias register to said first real register, said asserted data location field indicating that said first register value is in said first real register.

23. A processor system, comprising:

a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions including a first entry associated with a first instruction, said first entry identifying a first alias register containing a first register value for a first real register; and

an allocator to:

identify said first entry of said reorder buffer to be associated with a second instruction that is younger in order than said first instruction;

determine whether said first register value is valid for copying from said first alias register to said first real register;

copy said first register value from said first alias register to said first real register if it is determined that said first register value is valid; and

associate said first entry of said reorder buffer with said second instruction.

24. The processor system of claim 23, wherein said first entry of said first instruction includes a first valid data field to indicate whether said first register value is valid for copying from said first alias register to said first real register, and wherein said allocator reads said first valid data field to determine whether said first register value is valid.

25. The processor system of claim 24, wherein said allocator causes a deasserting of said first valid data field after determining that said first register value is valid for copying from said first alias register to said first real register.

26. The processor system of claim 23, further comprising:

a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry including a committed data location field to indicate whether a committed register value is in said first real register; and

wherein said allocator asserts said data location field after it is determined that said first register value is valid for copying from said first alias register to said first real register, said asserted data location field indicating that said first register value is in said first real register.

27. A computer readable medium comprising one or more software modules to:

provide a reorder buffer comprising a plurality of entries associated respectively with a plurality of instructions including a first entry associated with a first instruction, said first entry identifying a first alias register containing a first register value for a first real register;

identify said first entry of said reorder buffer to be associated with a second instruction that is younger in order than said first instruction;

determine whether said first register value is valid for copying from said first alias register to said first real register;

copy said first register value from said first alias register to said first real register if it is determined that said first register value is valid; and

associate said first entry of said reorder buffer with said second instruction.

28. The computer readable medium of claim 27, wherein said first entry of said first instruction includes a first valid data field to indicate whether said first register value is valid for

copying from said first alias register to said first real register, and wherein one or more software modules causes a reading of said first valid data field in determining whether said first register value is valid.

29. The computer readable medium of claim 28, wherein said one or more software modules causes a deasserting of said first valid data field after said first register value has been determined to be valid for copying from said first alias register to said first real register.

30. The computer readable medium of claim 27, wherein said one or more software modules:

provide a data commitment table comprising a plurality of entries associated respectively with a plurality of real registers including a first entry associated with said first real register, said first entry including a committed data location field to indicate whether a committed register value is in said first real register; and

asserts said data location field after it is determined that said first register value is valid for copying from said first alias register to said first real register, said asserted data location field indicating that said first register value is in said first real register.